

SN74LVC1G3157 Single-Pole Double-Throw Analog Switch

1 Features

- 1.65-V to 5.5-V V_{CC} Operation
- Useful for Both Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- Operating Frequency Typically 340 MHz at Room Temperature
- High Degree of Linearity
- High Speed, Typically 0.5 ns ($V_{CC} = 3\text{ V}$, $C_L = 50\text{ pF}$)
- Low ON-State Resistance, Typically $\approx 6\ \Omega$ ($V_{CC} = 4.5\text{ V}$)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Wearables
- Portable Computing
- Internet of Things
- Audio Signal Processing

3 Description

This single-pole double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G3157 device can handle both analog and digital signals. The SN74LVC1G3157 device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G3157DBV	SOT-23 (6)	2.90 mm × 1.60 mm
SN74LVC1G3157DCK	SC70 (6)	2.00 mm × 1.25 mm
SN74LVC1G3157DRL	SOT (6)	1.60 mm × 1.20 mm
SN74LVC1G3157DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G3157YZP	DSBGA (6)	1.41 mm × 0.91 mm
SN74LVC1G3157DSF	SON (6)	1.00 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

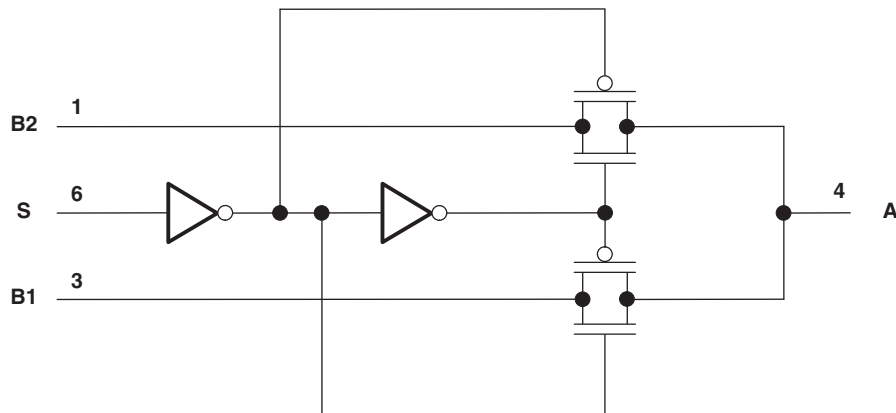


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4 Revision History

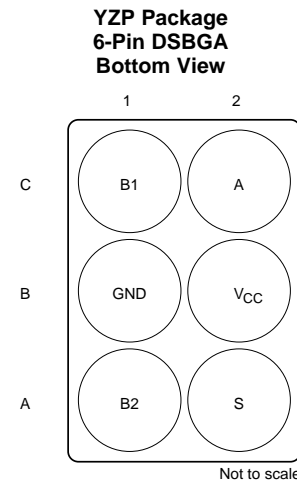
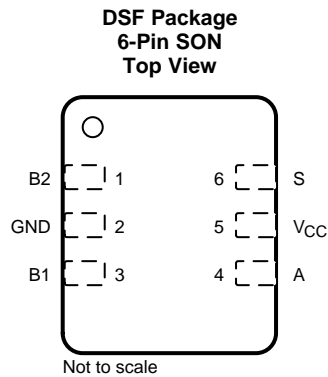
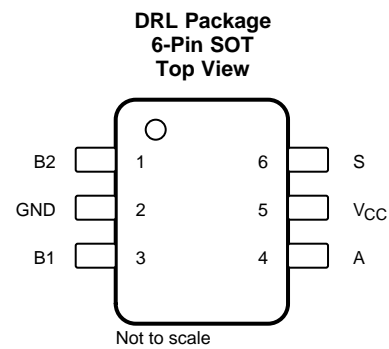
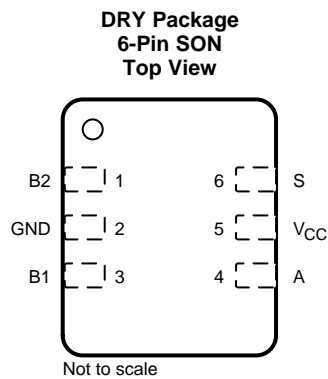
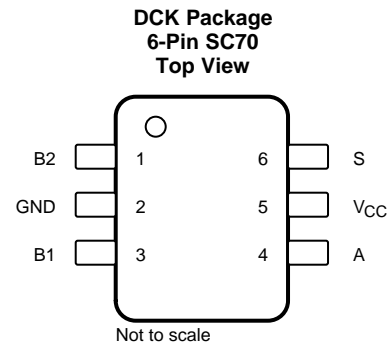
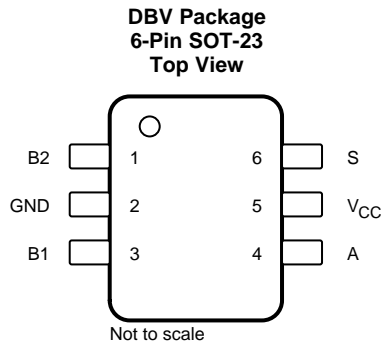
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (June 2015) to Revision J	Page
• Changed Operating Frequency from 300 MHz to 340 MHz throughout	1
• Deleted 200-V Machine Model (A115-A) from <i>Features</i>	1
• Updated <i>Device Information</i> table	1
• Updated pinout images for all packages	3
• Added temperature ranges for Storage temperature, T_{stg} and Junction temperature, T_J in <i>Absolute Maximum Ratings</i>	4
• Changed MAX value ± 1 to ± 0.1 for I_{off} and I_{IN} in <i>Electrical Characteristics</i> table	5

Changes from Revision H (May 2012) to Revision I	Page
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Updated document to new TI data sheet format	1
• Updated <i>Features</i>	1

Changes from Revision G (September 2011) to Revision H	Page
• Changed YZP with correct pin labels.	3
• Added <i>Thermal Information</i> table.	5
• Changed to correct Pin Label "S"	5

5 Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC70, SON, or SOT	DSBGA		
B2	1	A1	I/O	Switch I/O. Set S high to enable.
GND	2	B1	—	Ground
B1	3	C1	I/O	Switch I/O. Set S low to enable.
A	4	C2	I/O	Common terminal
V _{CC}	5	B2	—	Power supply
S	6	A2	I	Select

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		−0.5	6.5	V
V _{IN}	Control input voltage ⁽²⁾⁽³⁾		−0.5	6.5	V
V _{I/O}	Switch I/O voltage ⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Control input clamp current	V _{IN} < 0		−50	mA
I _{I/O}	I/O port diode current	V _{I/O} < 0 or V _{I/O} > V _{CC}		±50	mA
I _{I/O}	On-state switch current ⁽⁶⁾	V _{I/O} = 0 to V _{CC}		±128	mA
	Continuous current through V _{CC} or GND			±100	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for V_{I/O}.
- (6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for I_{I/O}.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	5.5	V
V _{I/O}	Switch input or output voltage	0	V _{CC}	V
V _{IN}	Control input voltage	0	5.5	V
V _{IH}	High-level input voltage, control input	V _{CC} = 1.65 V to 1.95 V	V _{CC} × 0.75	V
		V _{CC} = 2.3 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage, control input	V _{CC} = 1.65 V to 1.95 V	V _{CC} × 0.25	V
		V _{CC} = 2.3 V to 5.5 V	V _{CC} × 0.3	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.65 V to 1.95 V	20	ns/V
		V _{CC} = 2.3 V to 2.7 V	20	
		V _{CC} = 3 V to 3.6 V	10	
		V _{CC} = 4.5 V to 5.5 V	10	
T _A	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G3157					UNIT
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	YZP (DSBGA)	
	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA} Junction-to-ambient thermal resistance	165	259	142	234	123	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
r _{on}	ON-state switch resistance ⁽²⁾	See Figure 1 and Figure 2	V _I = 0 V	I _O = 4 mA	1.65 V	11	20	Ω
			V _I = 1.65 V	I _O = –4 mA		15	50	
			V _I = 0 V	I _O = 8 mA	2.3 V	8	12	
			V _I = 2.3 V	I _O = –8 mA		11	30	
			V _I = 0 V	I _O = 24 mA	3 V	7	9	
			V _I = 3 V	I _O = –24 mA		9	20	
			V _I = 0 V	I _O = 30 mA	4.5 V	6	7	
			V _I = 2.4 V	I _O = –30 mA		7	12	
			V _I = 4.5 V	I _O = –30 mA		7	15	
r _{range}	ON-state switch resistance over signal range ⁽²⁾⁽³⁾	0 ≤ V _{Bn} ≤ V _{CC} (see Figure 1 and Figure 2)	I _A = –4 mA	1.65 V			140	Ω
			I _A = –8 mA	2.3 V			45	
			I _A = –24 mA	3 V			18	
			I _A = –30 mA	4.5 V			10	
Δr _{on}	Difference of ON-state resistance between switches ⁽²⁾⁽⁴⁾⁽⁵⁾	See Figure 2	V _{Bn} = 1.15 V	I _A = –4 mA	1.65 V	0.5		Ω
			V _{Bn} = 1.6 V	I _A = –8 mA	2.3 V	0.1		
			V _{Bn} = 2.1 V	I _A = –24 mA	3 V	0.1		
			V _{Bn} = 3.15 V	I _A = –30 mA	4.5 V	0.1		
r _{on(flat)}	ON resistance flatness ⁽²⁾⁽⁴⁾⁽⁶⁾	0 ≤ V _{Bn} ≤ V _{CC}	I _A = –4 mA	1.65 V		110		Ω
			I _A = –8 mA	2.3 V		26		
			I _A = –24 mA	3 V		9		
			I _A = –30 mA	4.5 V		4		
I _{off} ⁽⁷⁾	OFF-state switch leakage current	0 ≤ V _I , V _O ≤ V _{CC} (see Figure 3)		1.65 V to 5.5 V		±1		μA
						±0.05	±0.1 ⁽¹⁾	
I _{S(on)}	ON-state switch leakage current	V _I = V _{CC} or GND, V _O = Open (see Figure 4)		5.5 V		±1		μA
						±0.1 ⁽¹⁾		
I _{IN}	Control input current	0 ≤ V _{IN} ≤ V _{CC}		0 V to 5.5 V		±1		μA
						±0.05	±0.1 ⁽¹⁾	
I _{CC}	Supply current	S = V _{CC} or GND		5.5 V		1	10	μA
ΔI _{CC}	Supply-current change	S = V _{CC} – 0.6 V		5.5 V			500	μA
C _i	Control input capacitance	S		5 V		2.7		pF

(1) T_A = 25°C

(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.

(3) Specified by design

(4) Δr_{on} = r_{on(max)} – r_{on(min)} measured at identical V_{CC}, temperature, and voltage levels

(5) This parameter is characterized, but not production tested.

(6) Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.

(7) I_{off} is the same as I_{S(off)} (off-state switch leakage current).

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
C _{io(off)}	Switch input/output capacitance	Bn		5 V		5.2		pF
C _{io(on)}	Switch input/output capacitance	Bn		5 V		17.3		pF
		A				17.3		

6.6 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	TYP	UNIT
Frequency response ⁽¹⁾ (switch on)	A or Bn	Bn or A	R _L = 50 Ω, f _{in} = sine wave (see Figure 6)	1.65 V	340	MHz
				2.3 V	340	
				3 V	340	
				4.5 V	340	
Crosstalk ⁽²⁾ (between switches)	B1 or B2	B2 or B1	R _L = 50 Ω, f _{in} = 10 MHz (sine wave) (see Figure 7)	1.65 V	–54	dB
				2.3 V	–54	
				3 V	–54	
				4.5 V	–54	
Feed through attenuation ⁽²⁾ (switch off)	A or Bn	Bn or A	C _L = 5 pF, R _L = 50 Ω, f _{in} = 10 MHz (sine wave) (see Figure 8)	1.65 V	–57	dB
				2.3 V	–57	
				3 V	–57	
				4.5 V	–57	
Charge injection ⁽³⁾	S	A	C _L = 0.1 nF, R _L = 1 MΩ (see Figure 9)	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	V _I = 0.5 V _{p-p} , R _L = 600 Ω, f _{in} = 600 Hz to 20 kHz (sine wave) (see Figure 10)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

(3) Specified by design

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5 and Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} ⁽¹⁾	A or Bn	Bn or A		2		1.2		0.8		0.3	ns
t _{en} ⁽²⁾	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
t _{dis} ⁽³⁾			3	13	2	7.5	1.5	5.3	0.8	3.8	
t _{B-M} ⁽⁴⁾			0.5		0.5		0.5		0.5		ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

(2) t_{en} is the slower of t_{PZL} or t_{PZH}.

(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.

(4) Specified by design.

6.8 Typical Characteristics

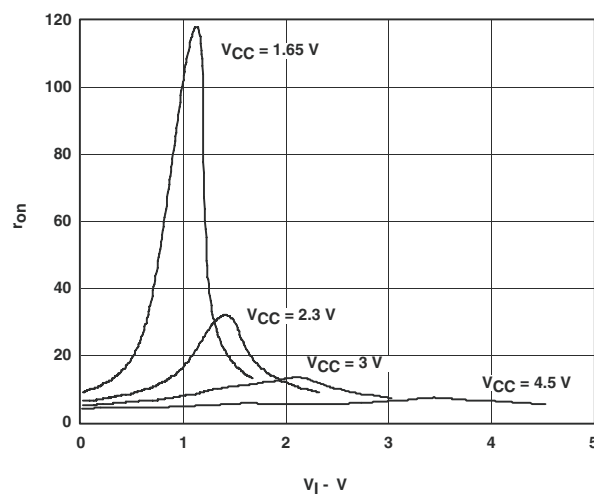


Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

7 Parameter Measurement Information

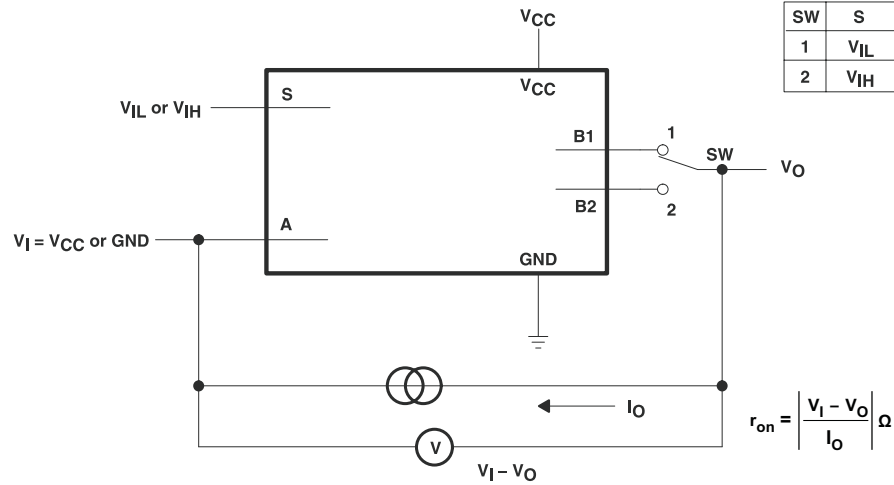


Figure 2. ON-State Resistance Test Circuit

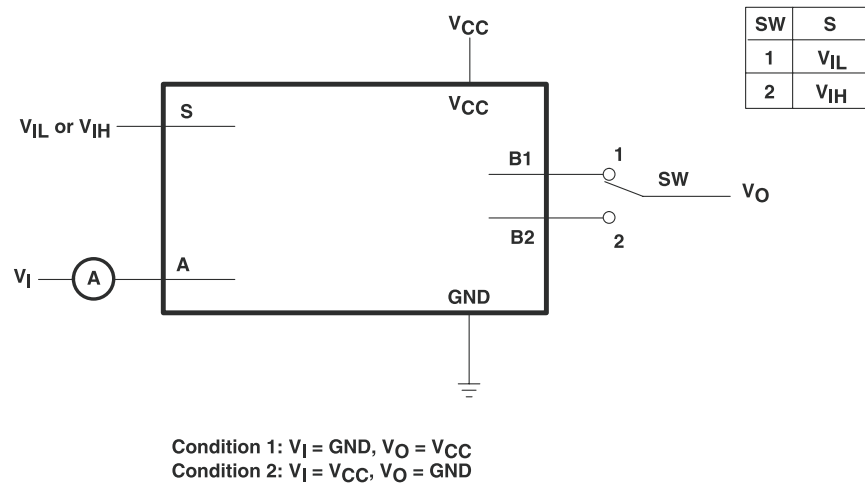


Figure 3. OFF-State Switch Leakage-Current Test Circuit

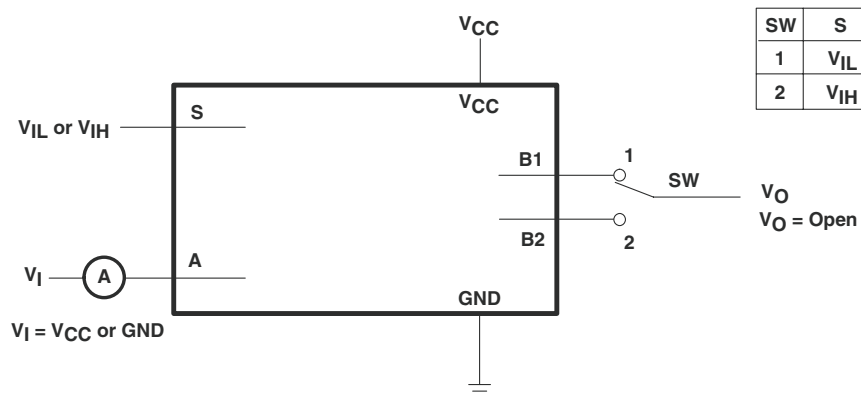
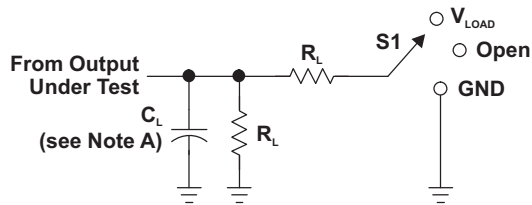


Figure 4. ON-State Switch Leakage-Current Test Circuit

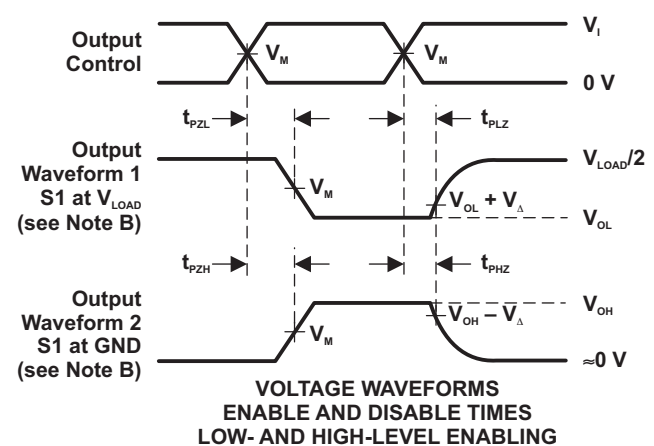
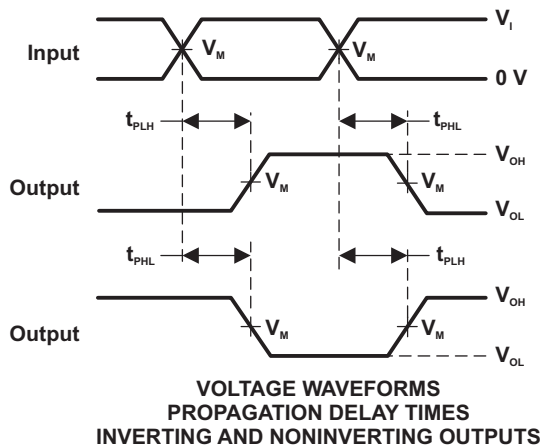
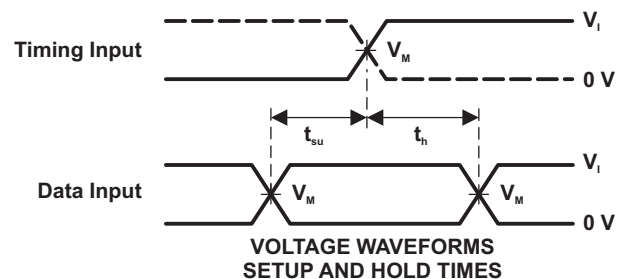
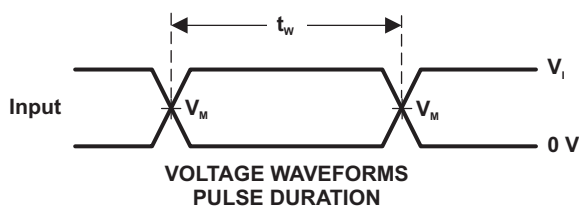
Parameter Measurement Information (continued)



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_A
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{on} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

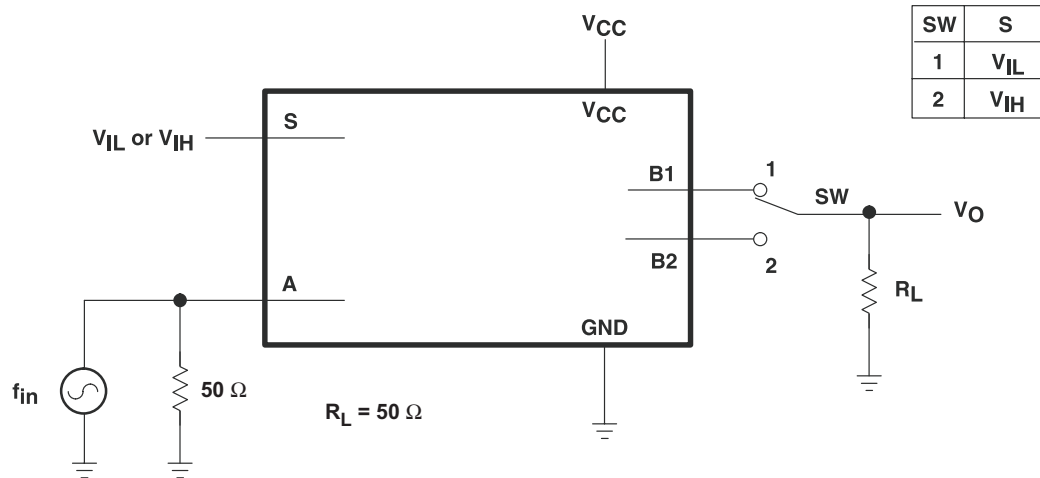


Figure 6. Frequency Response (Switch On)

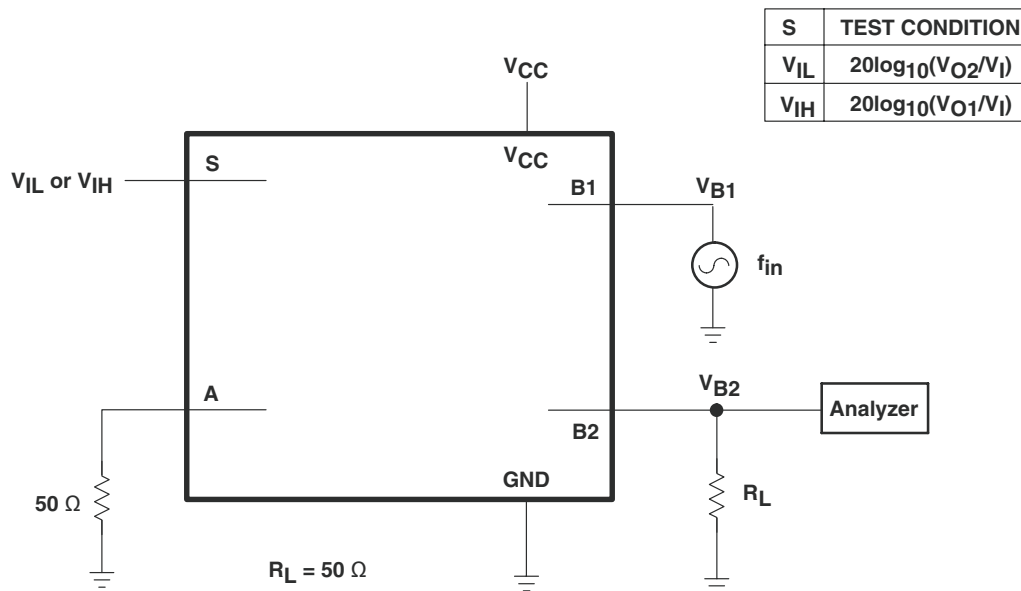


Figure 7. Crosstalk (Between Switches)

Parameter Measurement Information (continued)

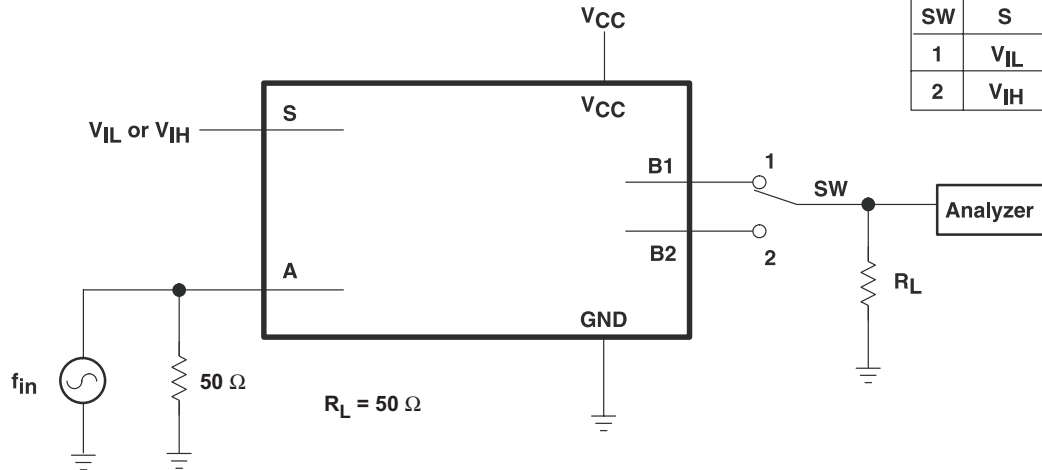


Figure 8. Feed Through

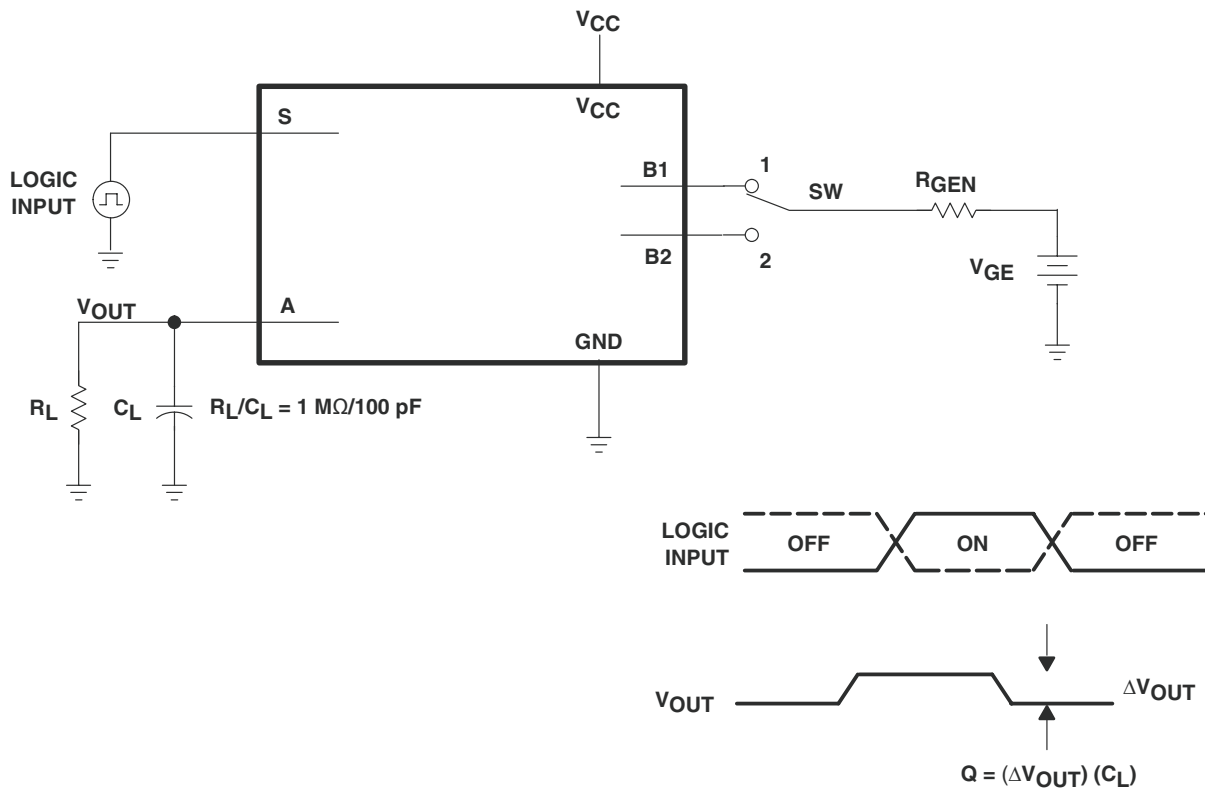


Figure 9. Charge-Injection Test

Parameter Measurement Information (continued)

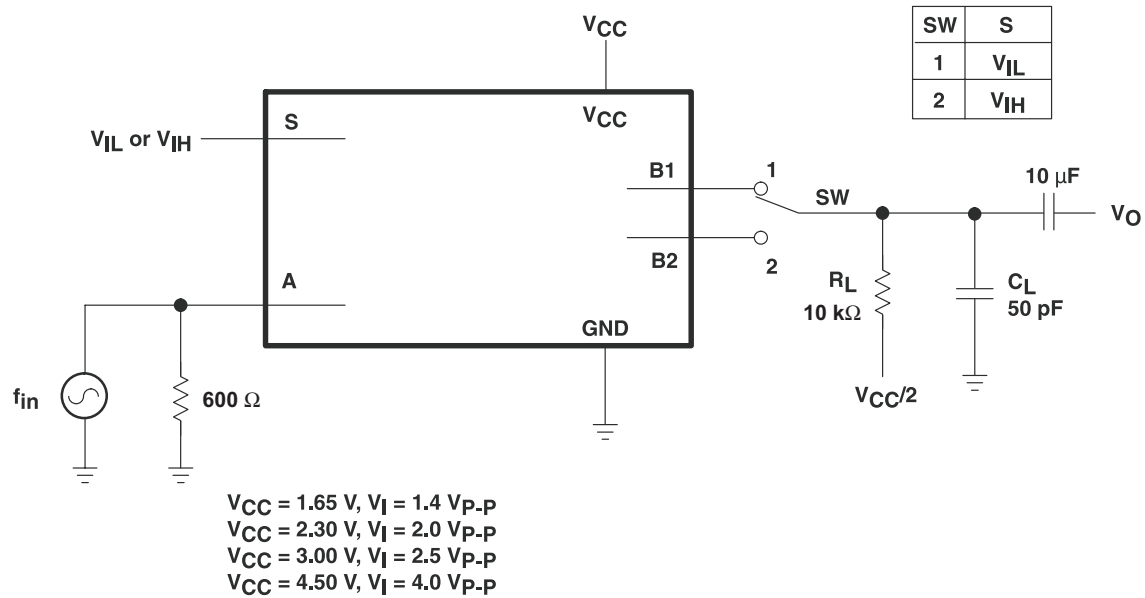


Figure 10. Total Harmonic Distortion

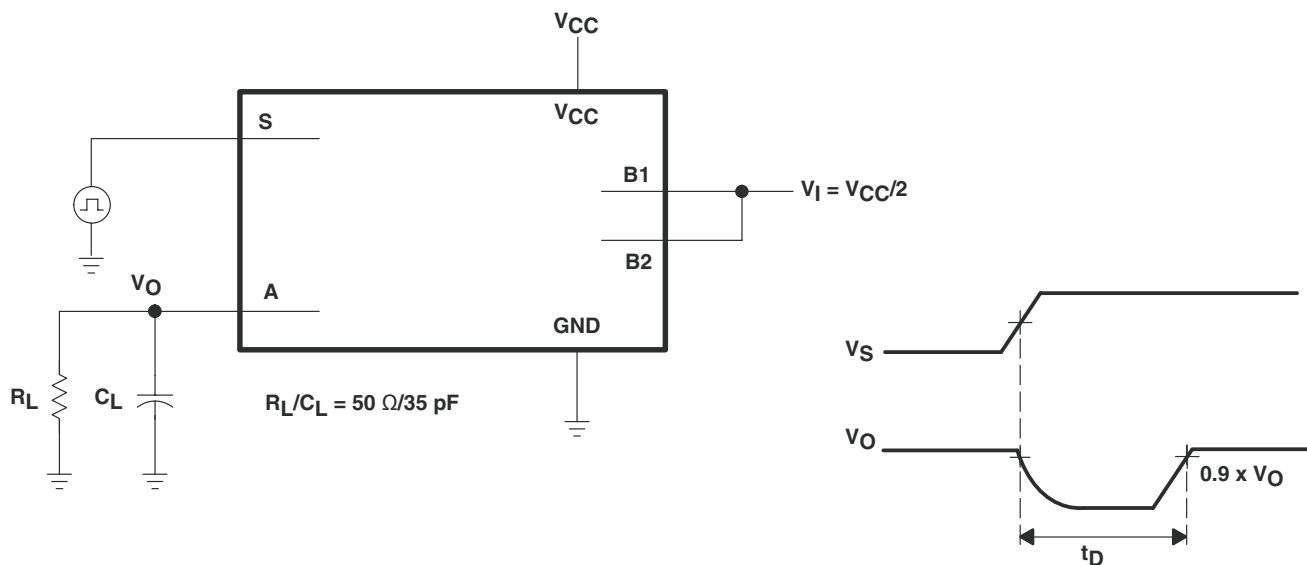


Figure 11. Break-Before-Make Internal Timing

8 Detailed Description

8.1 Overview

The SN74LVC1G3157 device is a single-pole double-throw (SPDT) analog switch designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

8.2 Functional Block Diagram

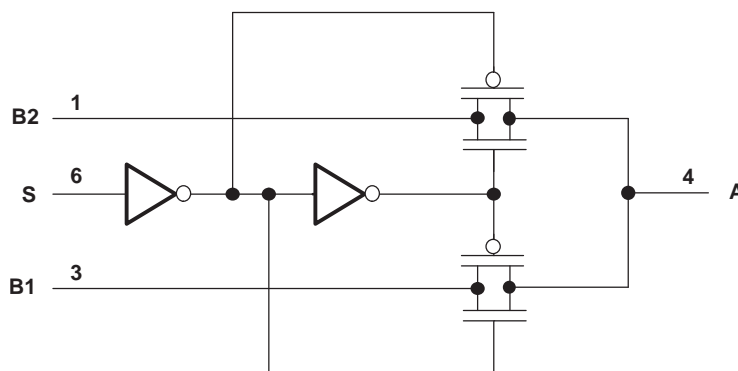


Figure 12. Logic Diagram (Positive Logic)

8.3 Feature Description

The 1.65-V to 5.5-V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

8.4 Device Functional Modes

Table 1 lists the ON channel when one of the control inputs is selected.

Table 1. Function Table

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G3157 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing, and so on. For details on the applications, see [SCYB014](#).

9.2 Typical Application

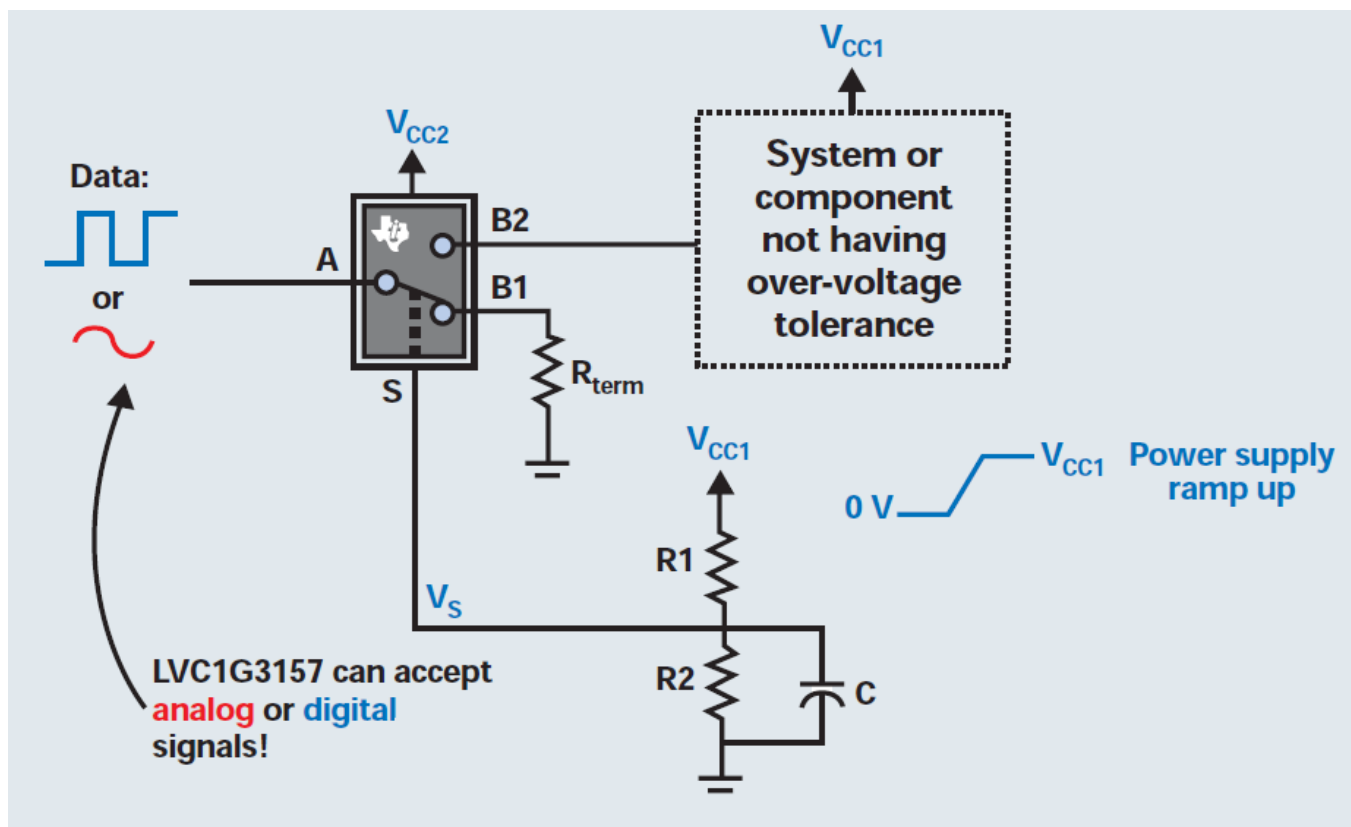


Figure 13. Typical Application Schematic

9.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until V_{CC} has ramped to a level in [Recommended Operating Conditions](#) before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2, and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use [Equation 1](#) to calculate the time required from a transition from ground (0 V) to half the supply voltage (VCC1/2).

$$\text{Set } \left(\frac{R_2}{R_1 + R_2} \times V_{CC1} > V_{IH} \right) \text{ of the select pin} \quad (1)$$

Choose Rs and C to achieve the desired delay.

When Vs goes high, the signal will be passed.

9.2.3 Application Curve

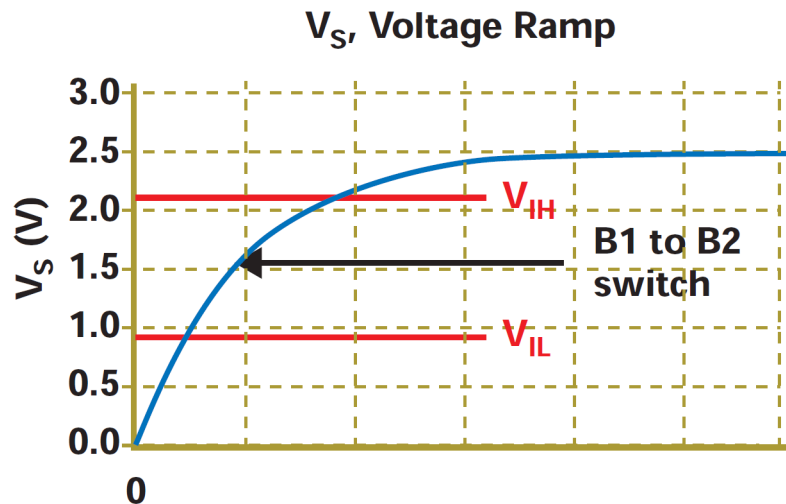


Figure 14. V_S Voltage Ramp

10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the V_{CC} pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

11 Layout

11.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either $50\ \Omega$ or $75\ \Omega$, as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

11.2 Layout Example

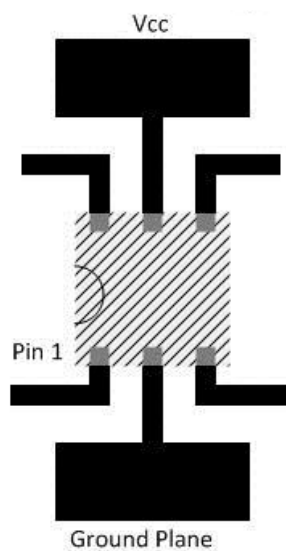


Figure 15. Recommended Layout Example